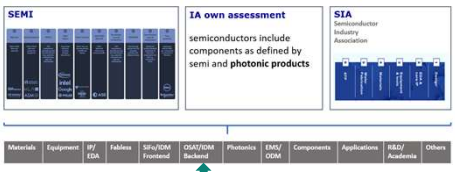
Industrial Alliance for Processors and Semiconductor Technologies

zvei electrifying ideas

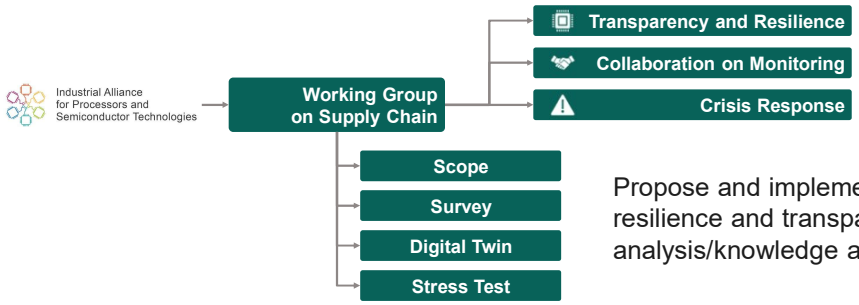
European Commission

Supply Chain Working Group

Cluster **OSAT/IDM Backend**



Objectives of the Supply Chain Working Group

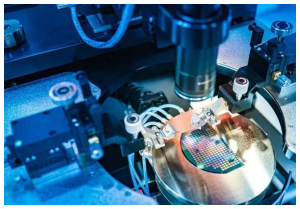


An industry working group working for the European industry on **End-to-End semiconductor*) supply chain and supply chains containing semiconductors**.

Join

Propose and implement measures to increase supply chain resilience and transparency, Support COM and ESB Board with analysis/knowledge and advise on possible future actions

Cluster OSAT[1)]/IDM[2)] Backend



Definition:

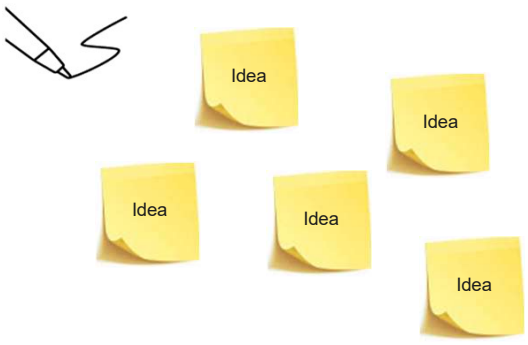
Covers assembly, packaging, and final test of chips—everything after wafer fab—spanning wafer bumping/singulation, die attach/wirebond/flip-chip, molding, substrate attach, advanced packaging and system-level/final test. Includes pure-play OSATs that provide outsourced services as well as IDMs/foundries with in-house/contracted back-end capacity

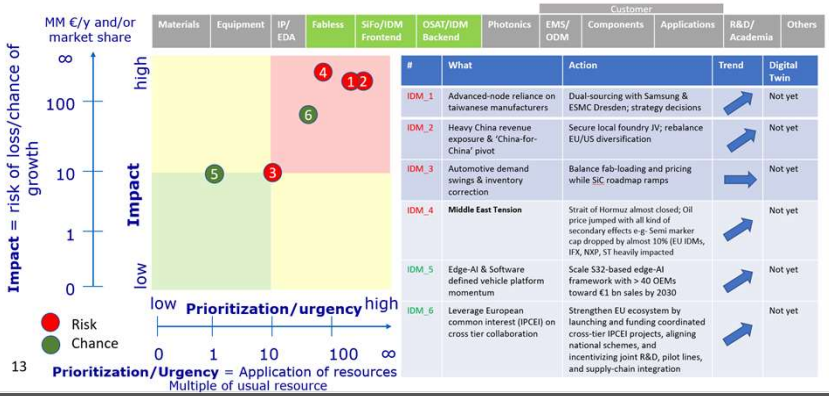
Pivotal actors in semiconductor OSAT[1)]/IDM[2)] Backend :

- Presto Engineering **[link]** — outsourced semiconductor test & manufacturing
- **STMicroelectronics [link] — Europe's largest back-end footprint; large packaging and test sites in Malta and Morocco**
- **Infineon Technologies [link] — integrated device manufacturer; substantial back-end assembly and test facilities**
- **Bosch (IDM) [link] — Automotive semiconductor and MEMS packaging/test centers**
- **NXP Semiconductors (IDM/fab-lite) [link] — Back-end and test center in Nijmegen (Netherlands)**
- TSMC **[link]** — foundry similar to an integrated device manufacturer and an advanced packaging leader central
- **Intel [link] — Foveros and Embedded Multi-die Interconnect Bridge advanced three-dimensional**
- ASE **[link]** — OSAT **[link]** ; assembly/test; advanced packaging (flip-chip, SiP, FO-WLP, 2.5D/3D)
- Silicon Box **[link]** — Advanced packaging foundry; high-density RDL, FO-WLP; chiplet integration
- STATS ChipPAC (JCET) **[link]** — OSAT; WLCSP/WLP; flip-chip; 2.5D/3D; test
- PalTech **[link]** — OSAT; memory packaging/test (DRAM/NAND); SiP
- Swissbit **[link]** — Industrial/embedded memory; secure storage modules; own back-end assembly

1) Outsourced Semiconductor Assembly and Test 2) Integrated Device Manufacturer

Feedback (on Definition, on companies, on actual Chance/Risk Matrix, on increasing resilience, on ...)





The TASK

- **Think about IDEAS & SUGGESTIONS to link the Base to the overall objectives**
- **Do some (silent) BRAINWRITING to put your Idea & Suggestion to a POST-IT**
- **Put your Post-it on the Poster with some EXPLANATORY WORDS to the group**
- **BRAINSTORM in the group about the ideas and make it as meaningful as possible**
- **PRESENT to the group (allow different opinions to be heard as well)**

- **Risk due to geopolitical situation in our domain and its supply chain mitigation strategy**
- **Risk due to complexity increase in our domain and its supply chain mitigation strategy**
- **Chances due to AI in our domain and how to accelerate harvesting the chances**
- **Chances due to collaboration in our domain and how to accelerate harvesting the chances**