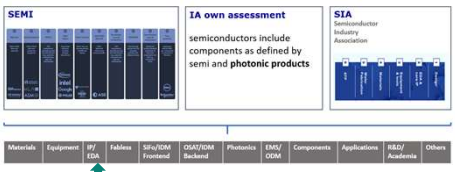
Industrial Alliance for Processors and Semiconductor Technologies

zvei electrifying ideas

European Commission

Supply Chain Working Group

Cluster IP/EDA



Objectives of the Supply Chain Working Group

Industrial Alliance for Processors and Semiconductor Technologies → **Working Group on Supply Chain**

- **Transparency and Resilience**
- **Collaboration on Monitoring**
- **Crisis Response**

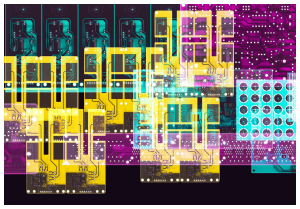
- **Scope**
- **Survey**
- **Digital Twin**
- **Stress Test**

An industry working group working for the European industry on **End-to-End semiconductor*) supply chain and supply chains containing semiconductors**.

Join

Propose and implement measures to increase supply chain resilience and transparency, Support COM and ESB Board with analysis/knowledge and advise on possible future actions

Cluster IP/EDA



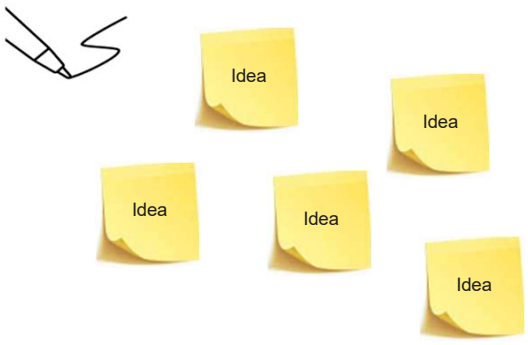
Definition:

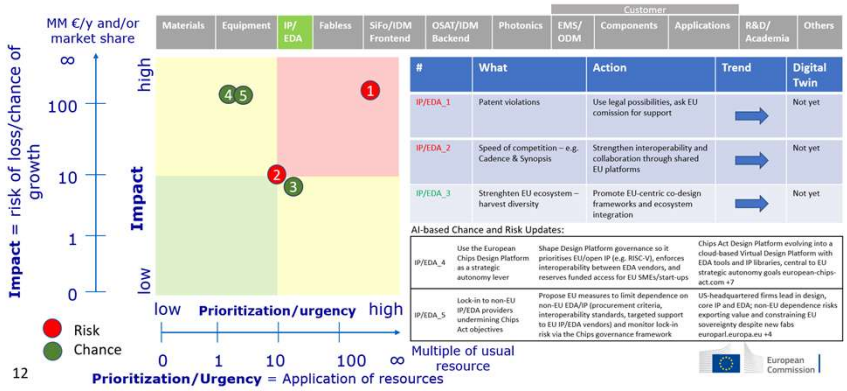
IP/EDA covers the software and reusable intellectual-property blocks used to design, verify, and sign off semiconductor devices—spanning logic/physical design, verification, packaging/system simulation, and licensable CPU/GPU/connectivity/security IP that SoC teams integrate to shorten time-to-market

Pivotal actors in semiconductor IP/EDA:

- Synopsys (incl. Ansys) [link] — #1 EDA + broad DesignWare IPCadence Design Systems
- **Siemens EDA (Mentor) [link] — Sign-off verification (Calibre) and DFT (Tessent)**
- Arm [link] — Dominant CPU IP licensor with license-and-royalty model; expanding across data-center/auto
- Codasip [link] — central processing unit intellectual property provider with configurable cores
- MunEDA [link] : EDA tools for analysis, optimization, and verification of analog, mixed-signal, and digital circuit designs
- Defacto Technologies [link] — delivers innovative register-transfer level platforms aimed at integration, verification
- Intento Design [link] : Focuses on analog and mixed-signal design acceleration, tools to automate circuit sizing and layout
- Celus [link] — a rising electronic design automation startup offering artificial-intelligence-driven printed circuit board design solutions
- Fraunhofer [link] — EDA research & design services; IP cores (audio codecs, DSP/RF, RISC-V)
- Cadence [link] — EDA (digital/analog, verification); interface IP (PCIe/DDR/USB/MIPI); Tensilica DSPs & 3D-IC

Feedback (on Definition, on companies, on actual Chance/Risk Matrix, on increasing resilience, on ...)





12

The TASK

- Think about IDEAS & SUGGESTIONS to link the Base to the overall objectives
- Do some (silent) BRAINWRITING to put your Idea & Suggestion to a POST-IT
- Put your Post-it on the Poster with some EXPLANATORY WORDS to the group
- BRAINSTORM in the group about the ideas and make it as meaningful as possible
- PRESENT to the group (allow different opinions to be heard as well)

- **Risk due to geopolitical situation in our domain and its supply chain mitigation strategy**
- **Risk due to complexity increase in our domain and its supply chain mitigation strategy**
- **Chances due to AI in our domain and how to accelerate harvesting the chances**
- **Chances due to collaboration in our domain and how to accelerate harvesting the chances**